## AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph at page 3, ls. 12-20, as follows:

-- Here, a related art example of the controller unit for processing in parallel the data transferred from the read channel unit will be illustrated in Fig. 19. As illustrated in Fig. 19, the controller unit 110 is provided with a PLL (Phase Locked Loop) circuit 111 for doubling the clock signal synchronized with the data and moreover is also provided with a parallel/serial converting unit 112 for converting the parallel data transferred from the read channel to the serial data, moreover, with addition of the shift register 113, mark detector 114, mark-interval counter 115 and data ~~modulator~~ demodulator 116. --